



발표자료 공유 안내

- Siemens EDA Keynote Session 을 포함한 오전 기조연설 자료는 공유가 불가능합니다.
- 아래 버튼을 통해 원하시는 자료를 선택해 주시면 취합 후 전달 드리도록 하겠습니다.

 [발표자료 요청하기](#)

Track	Session Title
Custom IC Design & Verification	<ul style="list-style-type: none"> • Exploring the Power of Solido’s AI-powered Environment: From Schematic to High-Sigma Verification • AI-Based Trimming and Optimization for Voltage Regulators: Proven Accuracy with Wafer Data • Engineering Tomorrow: Smart Verification Solutions with AI-Powered Solido Simulation Suite • Early Bug Detection and High-Confidence IP Sign-Off with the Solido IP Validation Suite
Digital IC Functional Design	<ul style="list-style-type: none"> • High Performance Connectivity IP from Alphawave: Accelerating Time To Market with Chiplet Reference Architecture • Enhancing Your SoC Debug & Optimization with Functional Monitoring
IC Physical Design & Verification	<ul style="list-style-type: none"> • AI-Driven DRC Debug at Samsung: Shift-Left with Calibre Vision AI and Recon Compare • Empowering design teams to deliver faster RTL-to-GDS design closure and better PPA with AI • Early Detection of ERC Violation with Calibre PERC CheckStore • Calibre new features and AI initiatives
IC Manufacturing & Test	<ul style="list-style-type: none"> • Calibre DFM Solutions or Design Analysis and Validation – Calibre LSG, Calibre mLFDD and Calibre SONR • Innovative streaming scan network (SSN) provides a generic data highway for the testing world • Scalable design-for-test (DFT) solutions from 2D IC to 3D IC • In-system Deterministic Test (IST) advancing in-field test quality
Board Design	<ul style="list-style-type: none"> • HyperLynx New features for 3DIC PKG & PCB design verification • Leveraging Digital Threads for Enhanced Efficiency, Security & Collaboration

- 개별 문의 세션 - 다음 세션에 대한 공유 요청은 직접 담당자에게 문의 부탁드립니다.

Track	Contact	Session Title
Custom IC Design & Verification	hoonkoo.lee@siemens.com	• LG Achieves Sign-Off at TSMC Advanced Node Using mPower Analog
	jungsin.choi@siemens.com	• Accelerating IC Design and Verification Productivity with Advanced Generative and Agentic AI
Digital IC Functional Design	jungsin.choi@siemens.com	• Transforming Electronic Design with Siemens EDA AI System
	kyeongjong.lim@siemens.com	• Designing Tomorrow’s Neural Networks with Today’s Tools – Edge AI with Catapult AI/N
	minsub.byun@siemens.com	• Empowering RTL Designers: Accurate Power Estimation and Optimization from Start to Finish
Digital IC Functional Verification	uiho.lee@siemens.com	<ul style="list-style-type: none"> • Tackling complexity early in the design cycle with Veloce CS and Innexis • Accelerate Innovation with the Veloce Ecosystem
	woojong.park@siemens.com	<ul style="list-style-type: none"> • From Buzz to Breakthroughs: AI-Powered Verification with Questa One • Questa One Avery VIP - Beyond the Verification IP
IC Physical Design & Verification	sangmok.rho@siemens.com	• Introduction to Calibre 3DSTACK Verification by Innovator3D IC Cockpit Including 3Dblox
Board Design	sw.lee@siemens.com	• Improving Design Productivity with AI-Infused Board Layout Tools
	rock.kim@siemens.com	• Introduction to the Methodology for Optimizing Connectivity Between Multi Boards Using Innovator3D IC

- 이 외 문의 사항은 행사 홈페이지 내 Q&A에 남겨 주시기 바랍니다.